ABSTRACT OF THE DISCLOSURE

The power semiconductor device includes a plurality of trenches disposed in a surface of a semiconductor active layer to reach a first base layer of a first conductivity type. The trenches are disposed at intervals to partition a main cell and a dummy cell. In the main cell, a second base layer of a second conductivity type and an emitter layer of the first conductivity type are disposed. In the dummy cell, a buffer layer of the second conductivity type is disposed. A gate electrode and gate insulating film are disposed in each trench. A partition structure is disposed in the surface of the semiconductor active layer to electrically isolate the buffer layer from the emitter electrode.